Automated Formal Synthesis of Wallace Tree Multipliers

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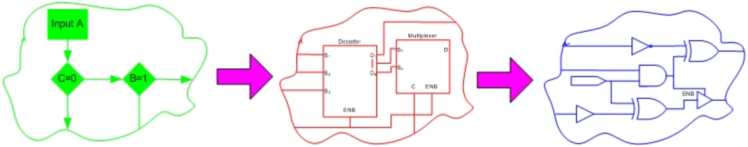
MWSCAS/NEWCAS, 2007

Outline

Hardware Synthesis

- Stepwise refinement of circuit descriptions from higher levels of abstraction to lower ones



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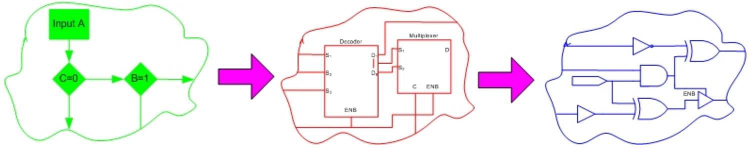

- Automated synthesis tools with sophisticated algorithms
    - Prone to design bugs

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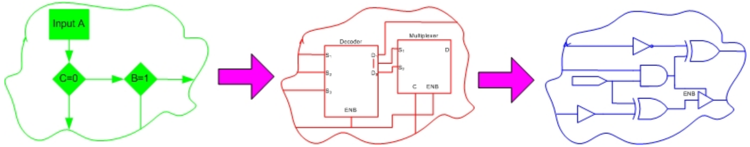

- Automated synthesis tools with sophisticated algorithms
  - Prone to design bugs

- Verification of synthesized results is a necessity
  - 70% of the design time and budget is spent on verification

Synthesis Verification

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Pre-Synthesis Verification

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Formal Synthesis

Synthesis is performed within a formal environment

- Most hardware systems can be handled
- Familiarity with formal semantics and reasoning

Proposed Solution

- Automated Formal Synthesis Approach
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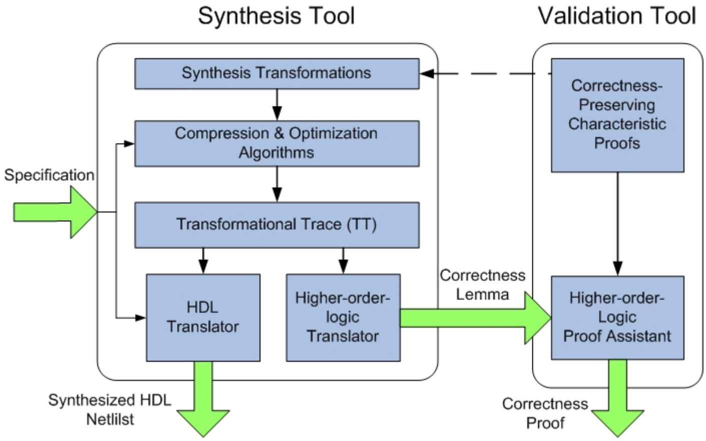
- Verification: Higher-Order-Logic Theorem Proving
  - Higher-Order-Logic
    - System of deduction with a precise semantics
    - High Expressiveness
  - Theorem Provers
    - Computer based proof tools

Methodology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Wallace Tree Multipliers

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- Using Full Adder (FA) and Half Adder (HA) cells

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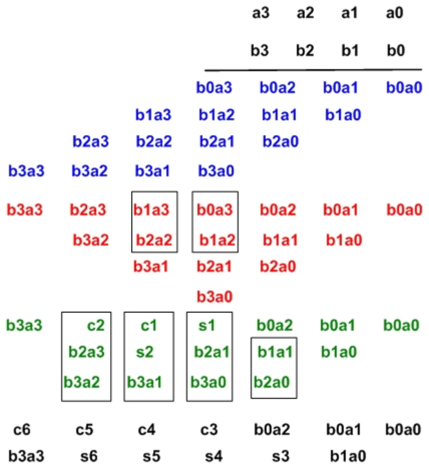

Automated Formal Synthesis of Wallace Tree Multipliers

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- Validation Tool
  - Isabelle/HOL
  - Accepts the correctness lemma
  - Returns True if the synthesis is complete and correct

Formalization of Wallace Tree Multipliers

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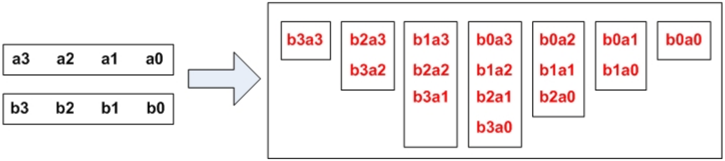
- `w_tree`: Generates a Wallace Tree



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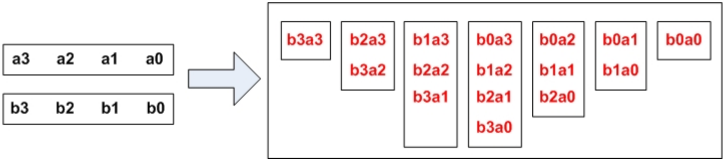
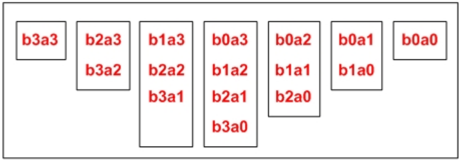


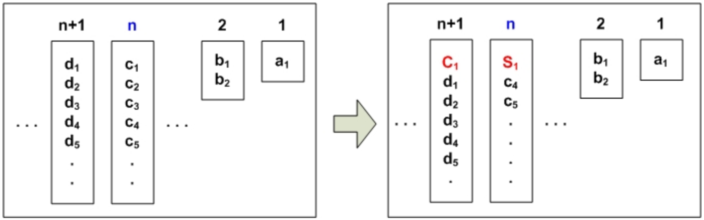
- `eval`: Computes integer value of a Wallace Tree



$$s_6 2^6 + s_5 2^5 + s_4 2^4 + s_3 2^3 + s_2 2^2 + s_1 2^1 + s_0 2^0$$

Formalization of Wallace Tree Transformations

- `fa_trans_tree`: FA transformation on a Wallace Tree



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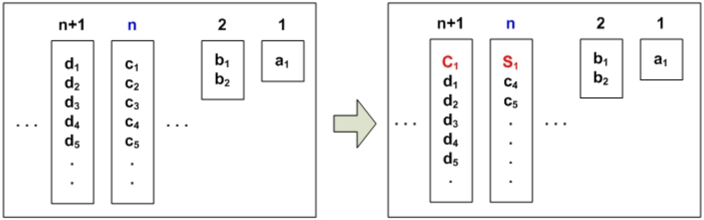
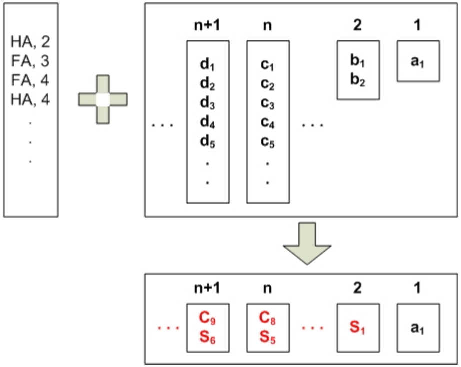


- Similar functions for the HA Transformation

Formalization of Wallace Tree Transformations

- apply_trans: Applies a sequence of FA and HA transformation to a Wallace Tree



Wallace Tree Multiplier Verification

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Theorem: FA transformation is correctness preserving

$\vdash \forall \mathtt{w}, \mathtt{n}.\ \mathtt{eval}(\mathtt{fa\_trans\_tree}\ \mathtt{w}\ \mathtt{n}) = \mathtt{eval}\ \mathtt{w}$

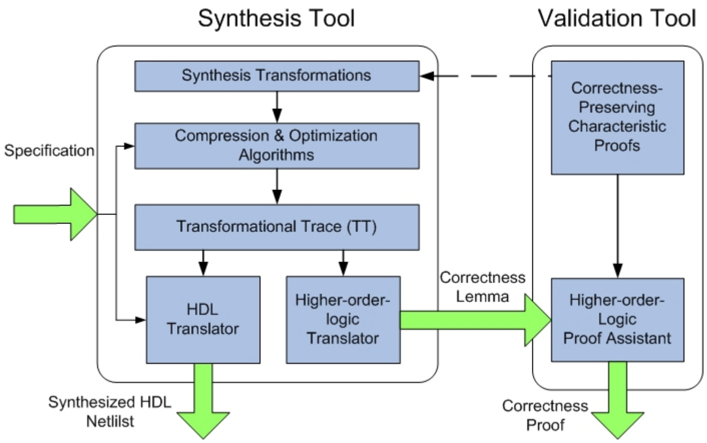
Theorem: HA transformation is correctness preserving

$\vdash \forall \mathtt{w}, \mathtt{n}.\ \mathtt{eval}(\mathtt{ha\_trans\_tree}\ \mathtt{w}\ \mathtt{n}) = \mathtt{eval}\ \mathtt{w}$

Theorem: Correctness of Wallace Tree synthesis

$\vdash \forall \mathtt{a}, \mathtt{b}, \mathtt{t}.\ \mathtt{eval}(\mathtt{apply\_trans}(\mathtt{w\_tree}\ \mathtt{a}\ \mathtt{b})\ \mathtt{t}) = \mathtt{a}_{10} * \mathtt{b}_{10}$

Synthesis of a MxN Multiplier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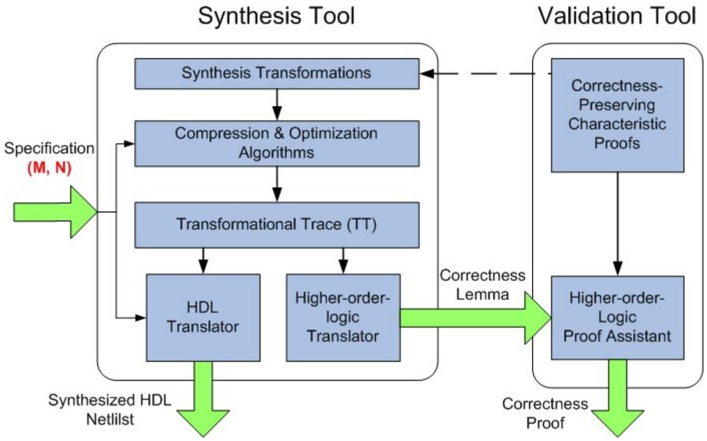
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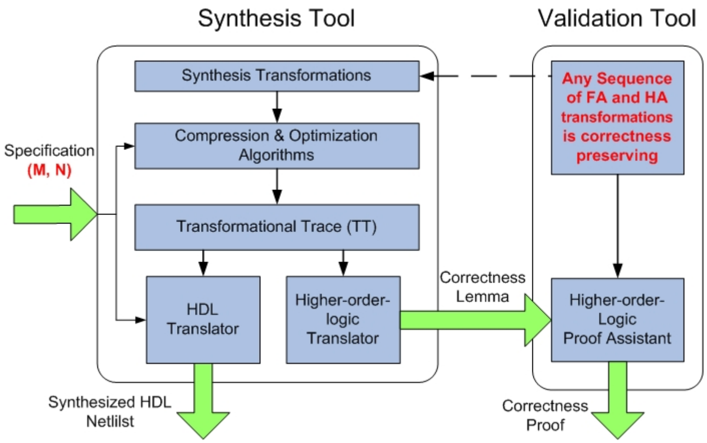
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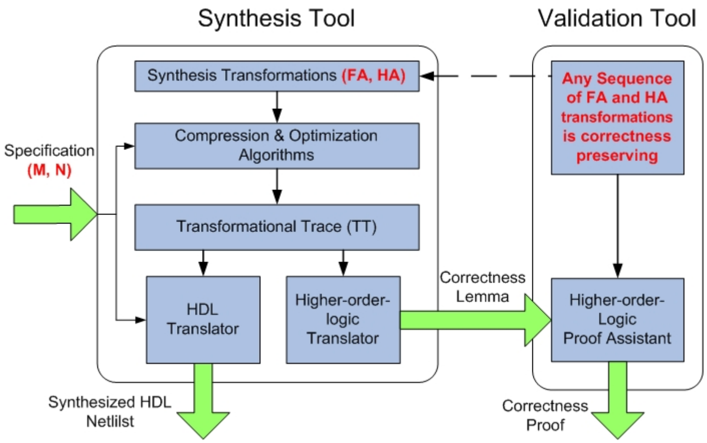
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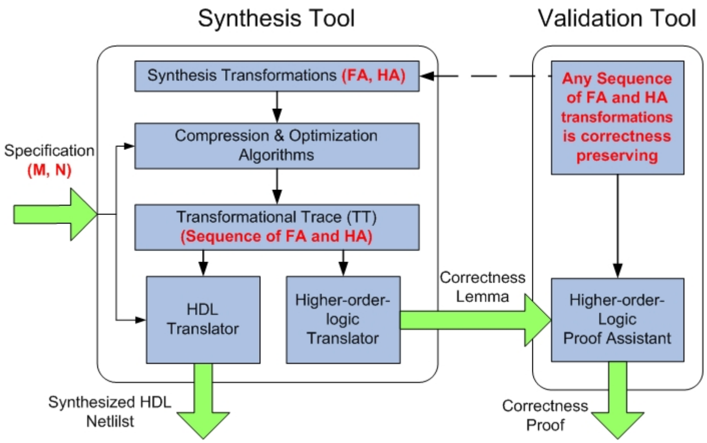
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  - Mechanically Verifying a family of multiplier circuits [Kapur, 1996]
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Formal synthesis has never been used with multipliers before

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- Future Work
  - Application to other digital circuits

More details and Isabelle/HOL sources

- Contact: o_hasan@ece.concordia.ca

Thank You!